WHAT IS CLAIMED IS:

1. A memory LSI defect analysis apparatus having a memory test system that performs electrical testing on memory LSI to be analyzed, the apparatus comprising:

a testing means for testing said memory LSI;

a data readout means for reading data of defect bits that is output from said testing means and holding the data in memory region of an analytical computer;

an address difference calculation means for calculating address differences between two pieces of defect data;

an address difference histogram production means for producing an address difference histogram based on said address differences;

an expected value function calculation means for calculating expected value function T(f) for factor f of an address difference based on said address difference histogram; and

a regular patterned defect mix rate calculation means for calculating mix rate of regular patterned defects included in a defect distribution from said expected value function.

2. A memory LSI defect analysis apparatus according to Claim 1, wherein said expected value function calculation means finds an expected value function T(f) for an address difference factor f based on said address difference histogram using equation:

$$T(f) = \frac{f\Sigma m(f)}{(N - ux)}$$

wherein

$\Sigma m(f)$: the number of combinations of defect bits where address difference has f as a factor;

N : total number of combinations of defect bits; and

ux : the number of combinations of defect bits where address

difference becomes 0.

3. A memory LSI defect analysis apparatus according to Claim 1, wherein said regular patterned defect mix rate calculation means comprises:

means for finding a maximum value T_{max} of expected value function T(f);

means for finding a value f_{max} of factor f at the time when said expected value function T(f) is at its maximum value T_{max};

means for determining whether or not said maximum value T_{max} is greater than 1, and when the value is greater than 1, deciding 'regular patterned distribution', and when the value is equal to or less than 1, deciding 'irregular patterned distribution'; and

means for finding a mix rate when there is regular patterned distribution using equation:

$$\text{regular patterned defect mix rate} = \sqrt{\frac{T\max-1}{f\max-1}}.$$

4. A memory LSI defect analysis apparatus having a memory test system that performs electrical testing on memory LSI to be analyzed, the apparatus comprising:

a testing means for testing said memory LSI;

a data readout means for reading data of defect bits that is output from said testing means and holding the data in memory region of an analytical computer;

an address difference calculation means for calculating address differences between two defect data;

an address difference histogram production means for producing an address difference histogram based on said address difference;

an expected value function calculation means for calculating

expected value function T(f) for factor f of an address difference based on said address difference histogram; and

a regular patterned defect mix rate function calculation means for finding a regular patterned defect mix rate for every factor f from expected value function T(f).

5. A memory LSI defect analysis apparatus according to Claim 4, further comprising a baseline compensation means for calculating a more accurate mix rate,

wherein said regular patterned defect mix rate function calculation means calculates regular patterned defect mix rate function corresponding to a baseline that has been compensated by said baseline compensation means.

6. A memory LSI defect analysis apparatus according to Claim 4, wherein said expected value function calculation means finds an expected value function T(f) for an address difference factor f based on said address difference histogram using equation:

$$T(f) = \frac{f\Sigma m(f)}{(N - ux)}$$

wherein

$\Sigma m(f)$: the number of combinations of defect bits where address difference has f as a factor;

N : total number of combinations of defect bits; and

ux : the number of combinations of defect bits where address difference becomes 0.

7. A memory LSI defect analysis apparatus according to Claim 4, wherein said regular patterned defect mix rate function calculation means comprises:

means for selecting a factor f and finding a value of expected value function T(f) for said factor f;

means for deciding whether or not the value of said expected value function T(f) is greater than 1, and when said value is greater than 1, assuming that defect distribution is regularly patterned at period f, then finding a value of regular patterned defect mix rate function MR(f) using equation:

$$MR(f) = \sqrt{\frac{T(f)-1}{f-1}};$$

means for, assuming that defect distribution is not regularly patterned at period f when the value of expected value function T(f) is equal to or less than 1, making the value of regular patterned defect mix rate function MR(f) equal to 0; and

means for controlling so that said regular patterned defect mix rate function MR(f) is found for every factor f.

8. A memory LSI defect analysis apparatus according to Claim 5, wherein said baseline compensation means performs compensation of a baseline during calculation of said regular patterned defect mix rate function MR(f); and

wherein said regular patterned defect mix rate function calculation means, which calculates regular patterned defect mix rate function MR(f) based on said compensation, comprising:

a defect number calculation means for finding total number of defects n;

means for selecting a factor f and finding a value of expected value function T(f) for said factor f;

means for deciding whether or not said expected value function T(f) is equal to or greater than $(n - f) / (n - 1)$ and the number of defects n is equal to or greater than factor f;

means for, assuming that defect distribution is regularly patterned at period f when conditions of $T(f) > (n - f) / (n - 1)$ and $n > f$ are met, finding a value of regular patterned defect mix rate function MR(f) using equation:

$$MR(f) = \sqrt{\frac{(n-1)T(f)-n+f}{n(f-1)}};$$

means for, assuming that defect distribution is not regularly patterned at period f when said conditions are not met, making regular patterned defect mix rate function MR(f) equal to zero; and

means for controlling so that said regular patterned defect mix rate function MR(f) is found for every factor f.

9. A memory LSI defect analysis apparatus according to Claim 8, wherein said baseline compensation means finds, when expected value function is found for the number of defects n of irregularly patterned defects, from the number of defect pairs $k(2n-fk-f)/2$ (wherein k is largest integer not exceeding n/f) where interval of address difference is a multiple of f, and from the number of combinations of defect pairs $n(n-1)/2$, regular patterned defect ratio P(f) at period f using equation:

$$P(f) = \frac{k(2n-fk-f)}{n(n-1)},$$

and calculates expected value function T(f) using equation:

$$T(f) = fP(f) = \frac{fk(2n-fk-f)}{n(n-1)}$$

in order to compensate expected value function T(f) based on the relationship to the number of defects n for factor f.

10. A memory LSI defect analysis method, comprising

a first step of testing a memory LSI;

a second step of reading data associated with defect bits which is

obtained from results of testing in said first step, and holding the data in a memory section of an analytical calculator;

a third step of calculating address differences between two pieces of defect data;

a fourth step of producing an address difference histogram based on said address differences;

a fifth step of calculating expected value function T(f) for factor f of an address difference based on said address difference histogram; and

a sixth step of calculating a regular patterned defect mix rate of a defect distribution from said expected value function.

11. A memory LSI defect analysis method according to Claim 10, wherein in said fifth step, based on said address difference histogram, expected value function T(f) relative to address difference factor f is found using equation:

$$T(f) = \frac{f\Sigma m(f)}{(N - ux)}$$

wherein

$\Sigma m(f)$: the number of combinations of defect bits where address difference has f as a factor;

N : total number of combinations of defect bits; and

ux : the number of combinations of defect bits where address difference becomes 0.

12. A memory LSI defect analysis method according to Claim 10, wherein said sixth step further comprising:

(a) a step of finding a maximum value T_{max} of expected value function T(f) in relation to address difference factor f;

(b) a step of finding a value f_{max} of factor f at the time when said expected value function T(f) is at its maximum value T_{max};

(c) a step of determining whether said maximum value T_{max} is larger than 1 or not;

(d) a step of deciding 'regular patterned distribution' when said maximum value T_{max} is greater than 1 and deciding 'irregular patterned distribution' when said maximum value is equal to or less than 1; and

(e) a step of finding a mix rate when there is regular patterned distribution using equation:

$$\text{regular patterned defect mix rate} = \sqrt{\frac{T\max-1}{f\max-1}}.$$

13. A memory LSI defect analysis method, comprising

a first step of testing a memory LSI;

a second step of reading data associated with defect bits which is obtained from results of testing in said first step, and holding the data in a memory section of an analytical calculator;

a third step of calculating address differences between two pieces of defect data;

a fourth step of producing an address difference histogram based on said address differences;

a fifth step of calculating expected value function T(f) for factor f of an address difference based on said address difference histogram; and

a sixth step of finding a regular patterned defect mix rate for every factor f from expected value function T(f).

14. A memory LSI defect analysis method according to Claim 13, further comprising:

a seventh step of compensating a baseline; and

an eighth step of calculating a regular patterned defect mix rate function based on said compensated baseline.

15. A memory LSI defect analysis method according to Claim 13, wherein in said fifth step, based on said address difference histogram, expected value function T(f) relative to address difference factor f is found using equation:

$$T(f) = \frac{f\Sigma m(f)}{(N-ux)}$$

wherein

$\Sigma m(f)$: the number of combinations of defect bits where address difference has f as a factor;

N : total number of combinations of defect bits; and

ux : the number of combinations of defect bits where address difference becomes 0.

16. A memory LSI defect analysis method according to Claim 13, wherein said sixth step further comprising:

(a) a step of selecting a factor f and finding a value of expected value function T(f) for said factor f;

(b) a step of deciding whether or not the value of expected value function T(f) exceeds 1;

(c) a step of deciding a defect distribution is regularly patterned at period f when the value of expected value function T(f) is greater than 1, and finding a value of regular patterned defect mix rate function MR(f) using equation:

$$MR(f) = \sqrt{\frac{T(f)-1}{f-1}};$$

(d) a step of deciding a defect distribution is not regularly patterned at period f when the value of expected value function T(f) is equal to or less than 1, and making the value of regular patterned defect mix rate function MR(f) equal to zero; and

(e) a step of checking whether regular patterned defect mix rate

function MR(f) has been found for every factor f, and if it is finished, then ending processing, and if it is not, then returning to said step (a).

17. A memory LSI defect analysis method according to Claim 14, wherein said eighth step further comprises:

(a) a step of finding total number of defects n;

(b) a step of selecting factor f;

(c) a step of finding a value of expected value function T(f) for said factor f, and deciding whether or not that value is equal to or greater than (n – f) / (n – 1) and the number of defects n is equal to or greater than factor f;

(d) a step of deciding defect distribution is regularly patterned at period f when conditions of T(f) > (n – f) / (n – 1) and n > f are met, and finding a value of regular patterned defect mix rate function MR(f) using equation:

$$MR(f) = \sqrt{\frac{(n-1)T(f)-n+f}{n(f-1)}};$$

(e) a step of deciding defect distribution is not regularly patterned at period f when said conditions are not met and making regular patterned defect mix rate function MR(f) equal to zero; and

(f) a step of checking whether regular patterned defect mix rate function MR(f) has been found for every factor f, and if it is finished, then ending processing, and if it is not, then returning to said step (b).

18. A memory LSI defect analysis method according to Claim 17, wherein said seventh step which performs baseline compensation, finds, when expected value function is found for number of defects n of

irregularly patterned defects, from the number of defect pairs k(2n–fk–f)/2 (wherein k is largest integer not exceeding n/f) where interval of address difference is a multiple of f, and from the number of combinations of defect pairs n(n–1)/2, regular patterned defect ratio P(f) at period f using equation:

$$P(f) = \frac{k(2n - fk - f)}{n(n-1)},$$

and calculates expected value function T(f) using equation:

$$T(f) = fP(f) = \frac{fk(2n - fk - f)}{n(n-1)}$$

in order to compensate expected value function T(f) based on the relationship to the number of defects n for factor f.

19. A computer program product comprising a computer usable medium having computer readable program code means embodied in said medium for performing electrical testing on memory LSI to be analyzed, by a computer having a memory LSI defect analysis apparatus that comprises a memory test system, said product comprising;

a first computer readable program code means for reading data that is obtained as a result of said testing and holding the data in memory region of an analytic calculator;

a second computer readable program code means for calculating address differences between two pieces of defect data;

a third computer readable program code means for producing an address difference histogram based on said address difference;

a fourth computer readable program code means for calculating expected value function T(f) for factor f of an address difference based on said address difference histogram; and

a fifth computer readable program code means for calculating mix rate of regular patterned defects included in a defect distribution from

said expected value function.

20. A computer program product according to Claim 19, wherein said fifth computer readable program code means includes a sixth computer readable program code means for finding a regular patterned defect mix rate for every factor f.

21. A computer program product according to Claim 20, further comprising:

a seventh computer readable program code means for performing baseline compensation; and

an eight computer readable program code means for calculating a regular patterned defect mix rate function based on said compensated baseline.

22. A computer program product according to Claim 19, wherein said fourth computer readable program code means finds expected value function T(f) for factor f of an address difference based on said address difference histogram using equation:

$$T(f) = \frac{f\Sigma m(f)}{(N - ux)}$$

wherein

$\Sigma m(f)$: the number of combinations of defect bits where address difference has f as a factor;

N : total number of combinations of defect bits; and

ux : the number of combinations of defect bits where address difference becomes 0.

23. A computer program product according to Claim 19, wherein said fifth computer readable program code means further comprising:

(a) computer readable program code means for finding a maximum value T_{max} of expected value function T(f) in relation to address difference factor f;

(b) computer readable program code means for finding a value f_{max} of factor f at the time when said expected value function T(f) is at its maximum value T_{max};

(c) computer readable program code means for deciding whether or not said maximum value T_{max} is larger than 1;

(d) computer readable program code means for deciding 'regular patterned distribution' when said maximum value is greater than 1, and deciding 'irregular patterned distribution' when said maximum value is equal to or less than 1; and

(e) computer readable program code means for finding a mix rate when there is regular patterned distribution using equation:

$$\text{regular patterned defect mix rate} = \sqrt{\frac{T\max - 1}{f\max - 1}}.$$

24. A computer program product according to Claim 20, wherein said sixth computer readable program code means further comprising:

(a) computer readable program code means for selecting factor f and finding a value of expected value function T(f) for said factor f;

(b) computer readable program code means for deciding whether or not the value of said expected value function T(f) exceeds 1;

(c) computer readable program code means for deciding a defect distribution is regularly patterned at period f when the value of expected value function T(f) is greater than 1, and finding a value of regular patterned defect mix rate function MR(f) using equation:

$$MR(f) = \sqrt{\frac{T(f)-1}{f-1}};$$

(d) computer readable program code means for deciding a defect distribution is not regularly patterned at period f when the value of expected value function T(f) is equal to or less than 1, and making regular patterned defect mix rate function MR(f) equal to zero; and

(e) computer readable program code means for checking whether regular patterned defect mix rate function MR(f) has been found for every factor f, and if it is finished then ending processing, and if it is not then returning to said process (a).

25. A computer program product according to Claim 20, wherein said eighth computer readable program code means further comprising:

(a) computer readable program code means for finding total number of defects n;

(b) computer readable program code means for selecting factor f;

(c) computer readable program code means for finding the value of expected value function T(f) for said factor f, and deciding whether or not said value is equal to or greater than (n – f) / (n – 1) and the number of defects n is equal to or greater than factor f;

(d) computer readable program code means for deciding defect distribution is regularly patterned at period f when conditions of T(f) > (n – f) / (n – 1) and n > f are met, and finding a value of regular patterned defect mix rate function MR(f) using equation:

$$MR(f) = \sqrt{\frac{(n-1)T(f)-n+f}{n(f-1)}};$$

(e) computer readable program code means for deciding defect

distribution is irregularly patterned at period f when said conditions are not met and making regular patterned defect mix rate function MR(f) equal to zero; and

(f) computer readable program code means for checking whether regular patterned defect mix rate function MR(f) has been found for every factor f, and if it is finished then ending processing, and if it is not then returning to said process (b).

26. A computer program product according to Claim 21, wherein said seventh computer readable program code means finds, when expected value function is found for the number of defects n of irregularly patterned defects, from the number of defect pairs k(2n–fk–f)/2 (wherein k is largest integer not exceeding n/f) where interval of address difference is a multiple of f, and from the number of combinations of defect pairs n(n–1)/2, regular patterned defect ratio P(f) at period f using equation:

$$P(f) = \frac{k(2n - fk - f)}{n(n-1)}, \text{ and}$$

calculates expected value function T(f) using equation:

$$T(f) = fP(f) = \frac{fk(2n - fk - f)}{n(n-1)}$$

in order to compensate expected value function T(f) based on the relationship to the number of defects n for factor f.